



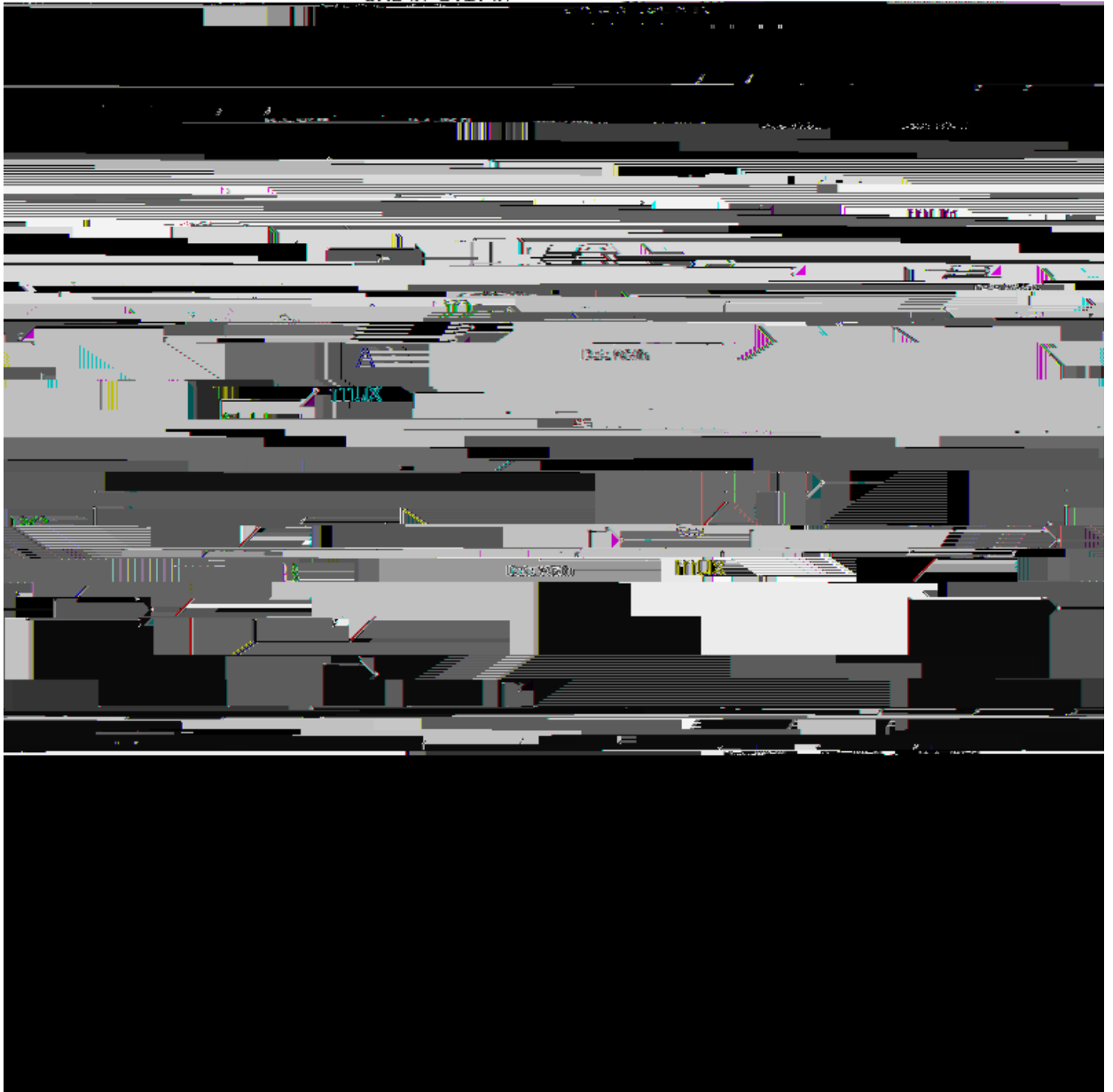


Fig. 2.

The first figure corresponds to PC implemented in general purpose register block, and the second – to PC implemented as a standalone register. The first variant requires less hardware resources but it is almost 2 times slower then the second variant. Register blocks RG A and RG B contain

| Type /     | 12 bit | 16 bit | 24 bit | 32 bit |
|------------|--------|--------|--------|--------|
| Data Width |        |        |        |        |

| Condition code | Mnemonic | Meaning |
|----------------|----------|---------|
|----------------|----------|---------|

|         |          |   |   |   |   |   |
|---------|----------|---|---|---|---|---|
| Bit     | 5...     | 4 | 3 | 2 | 1 | 0 |
| Meaning | Reserved | I | C | O | N | Z |

The screenshot displays the LTspice simulation environment. At the top, a parameter table is visible with columns for 'Parameter' and 'Value'. Below this, a circuit schematic is shown, featuring a MOSFET model (M1) and various passive components. The main area of the image is occupied by a multi-trace waveform plot. The plot shows several signals over time, with a time scale of 100ns. The signals include a square wave input, a MOSFET gate voltage, a MOSFET drain current, and a MOSFET drain voltage. The plot is titled 'M1' and 'M2'.

