2

- WBW_FIFO signals

Signal name	Size	Direction

pciw_renable_in	1	I	PCIW_FIFO's read enable input. When FIFO is not empty and read enable is high, data provided on data outputs will change to next written location on rising WB clock edge.

			Indicates that at least one unfinished
pcir_transaction_ready_out	1	O	