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Fig. 2 Block diagram of multipli951.191.96242 560.027/ 758.96037 Tm( )TjETEt3multipli951.191s7/ 75

1. Introduction

The design of the All Digital FM Receiver circuit in this project uses Phase Locked Loop (PLL) as the main core. The task of the PLL is to maintain coherence between the input (modul

For this algorithm, as shown in Fig. 3, the individual partial products determined from the multiplicand may be: added to, subtracted to, or may not change the final product at all b

frequency changes of the input signal once it is locked, hence it can be act as FM demodulator in receiver system.

Another means of describing the operation of the PLL is to observe that the

Timing Summary:

We conclude that the normalized circuit area is 13,835/6 = 2,306 gates

5. Appealing Point and Originality

The architecture used in this design has been explained in

```
    if (input2(5)='1') then
    if (input2(4)='1') then
    part5 <= (others => '0');
```

```
101 => "01101000",
102 => "01101000",
103 => "01100111",
104 => "01100111",
105 => "01100110",
106 => "01100110",
107 => "01100101",
108 => "01100101",
109 => "01100100",
110 => "01100100",
111 => "01100011",
```

```
      reset : IN     std_logic ;
      c     : IN     signed (7 DOWNTO 0);
      d1    : OUT    signed (11 DOWNTO 0);
      d2    : OUT    signed (11 DOWNTO 0)
   );
END COMPONENT;
COMPONENT nco
PORT (clk   : IN     std_logic ;
      reset : IN     std_logic ;
      din   : IN     signed (11 DOWNTO 0);
      dout  : OUT    signed (7 DOWNTO 0)
   );
END COMPONENT;
```

```
SIGNAL clk : std_logic := '0' ;
SIGNAL reset : std_logic := '1';
SIGNAL fmin : std_logic_vector(7 downto 0);
SIGNAL dmout : std_logic_vector(11 downto 0);
constant clkperiod : time := 62.5 ns;

BEGIN
       uut: circuit PORT MAP(
              clk => clk,
              reset => reset,
              fmin => fmin,
              dmout => dmout
            );

    RESET_GEN: process
    begin
```

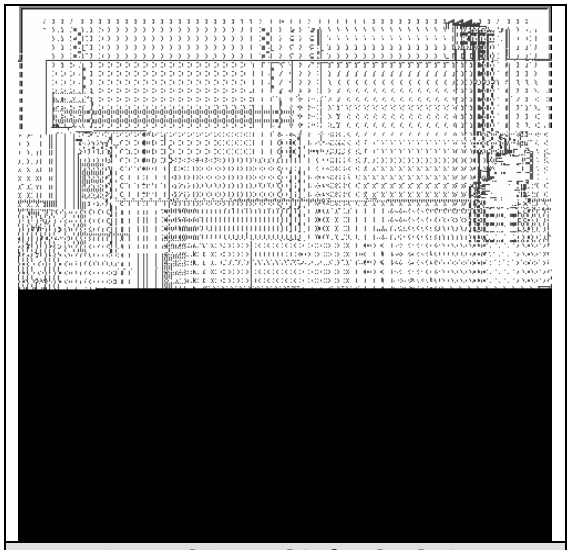

Fig. 13 Chip graphic for the design

ChipScope Pro 6.3i provides an integrated logic analyzer used to capture data in the designed circuit. After design is downloaded to FPGA board, ChipScope Pro will trigger input data and capture the output data via parallel cable in JTAG Boundary Scan mode as shown in Fig. 14. Captured data is in the listing form of 12-bit binary number as shown in Fig. 15. We can adjust how many samples needed to be captured; here we captured 1024 samples output data, then we plot it by ModelSim to obtain the actual demodulated signal view as shown in Fig.16

Appendix: